IN THE CLAIMS

1. (original): A stacked semiconductor device, comprising:

a first substrate that has external connecting terminals;

first terminals that are placed on a surface of the first substrate opposite to a surface of the first substrate on which the external connecting terminals of the first substrate are formed;

at least one first semiconductor chip that is mounted on the first substrate;

a second substrate that is placed on the first semiconductor chip;

at least one second semiconductor chip that is mounted on the second substrate; and

second terminals that are formed on the second substrate and electrically connected to at least one of the first semiconductor chip and the second semiconductor chip, the second terminals being connected to the first terminals by wire bonding.

2. (original): The stacked semiconductor device as claimed in claim 1, wherein:

the second semiconductor chip is attached to the first terminals of the first substrate by wire bonding;

the first semiconductor chip is mounted on the second substrate by flip-chip bonding; and

the second terminals of the second substrate are connected to the first terminals of the first substrate by wire bonding.

3. (original): The stacked semiconductor device as claimed in claim 2, wherein:

the second substrate has an extending portion that extends beyond an outer periphery of the second semiconductor chip;

the second terminals of the second substrate are bonding pads formed at the extending portion; and

the second terminals are connected to the first terminals by wire bonding.

4. (original): The stacked semiconductor device as claimed in claim 3, wherein:

the extending portion of the second substrate has notches; and

bonding wires that connect the second semiconductor chip to the first terminals of the first substrate extend through the notches.

5. (original): The stacked semiconductor device as claimed in claim I, wherein:

the first semiconductor chip is connected to the first terminals of the first substrate by wire bonding;

the second semiconductor chip is connected to the second terminals of the second substrate by wire bonding; and

the second terminals of the second substrate are connected to the first terminals of the first substrate by wire bonding.

6. (original): The stacked semiconductor device as claimed in claim 5, wherein:

the second substrate has an extending portion that extends beyond an outer periphery of the second semiconductor chip; and

the second terminals of the second substrate are connected to the first terminals of the first substrate by wire bonding via first bonding pads formed at the extending portion.

7. (original): The stacked semiconductor device as claimed in claim 6, wherein:

the second semiconductor chip is connected by wire bonding to second bonding pads formed on the second substrate; and

the second bonding pads are connected to the first bonding pads via a wiring pattern formed on the second substrate.

8. (original): The stacked semiconductor device as claimed in claim 1, wherein the second substrate has an extending portion extending toward a periphery of the second substrate, and the extending portion has an end surface that is exposed in a side surface of the packaged semiconductor device.

9. (original): The stacked semiconductor device as claimed in claim 8, wherein the end surface of the extending portion is a cut surface formed by cutting so as to individualize the stacked semiconductor device.

10. (original): The stacked semiconductor device as claimed in claim 1, wherein a conductive layer is provided on a substantially entire surface of the second substrate opposite to a surface provided with the second terminals.

11. (new): In a stacked semiconductor device connectable to an external device; wherein the stacked semiconductor device includes

a lower circuit board including external connecting terminals on a lower surface of the lower circuit board, for connecting the stacked semiconductor device to the external device, and first wire bonding terminals on an upper surface of the lower circuit board, the first wire bonding terminals being electrically connected to the external connecting terminals through the lower circuit board,

at least one first semiconductor chip that is mounted on the upper surface of the lower circuit board, and

at least one second semiconductor chip that is mounted above the upper surface of the circuit board and above the first semiconductor chip;

the improvement comprising:

an upper circuit board mounted between the first semiconductor chip and the second semiconductor chip, such that a lower surface of the upper circuit board is in contact with the first semiconductor device and an upper surface of the upper circuit board is in contact with the second semiconductor device; wherein

the upper circuit board includes second wire bonding terminals which are electrically connected, through the upper circuit board, to electrodes of at least one of the first semiconductor chip and the second semiconductor chip; and wherein

the second wire bonding terminals and the first wire bonding terminals are connected by wire bonding;

whereby at least one of the first semiconductor chip and the second semiconductor chip is electrically connected to the external connecting terminals on the lower surface of the lower circuit board.

12. (new): The stacked semiconductor device as claimed in claim 11, wherein:

the second semiconductor chip is attached to the first wire bonding terminals of the lower circuit board by wire bonding;

the first semiconductor chip is mounted on the upper circuit board by flip-chip bonding; and

the second wire bonding terminals of the upper circuit board are connected to the first wire bonding terminals of the lower circuit board by wire bonding.

13. (new): The stacked semiconductor device as claimed in claim 12, wherein:

the upper circuit board comprises an extending portion that extends beyond an outer periphery of the second semiconductor chip;

the second wire bonding terminals of the upper circuit board are bonding pads formed at the extending portion; and

the second wire bonding terminals are connected to the first wire bonding terminals by wire bonding.

14. (new): The stacked semiconductor device as claimed in claim 13, wherein:

the extending portion of the upper circuit board comprises notches; and

bonding wires that connect the second semiconductor chip to the first wire bonding terminals of the lower circuit board extend through the notches.

15. (new): The stacked semiconductor device as claimed in claim 11, wherein:

the first semiconductor chip is connected to the first wire bonding terminals of the lower circuit board by wire bonding;

the second semiconductor chip is connected to the second wire bonding terminals of the upper circuit board by wire bonding; and

the second wire bonding terminals of the upper circuit board are connected to the first wire bonding terminals of the lower circuit board by wire bonding.

16. (new): The stacked semiconductor device as claimed in claim 15, wherein:

the upper circuit board comprises an extending portion that extends beyond an outer periphery of the second semiconductor chip; and

the second wire bonding terminals of the upper circuit board are connected to the first wire bonding terminals of the lower circuit board by wire bonding via first bonding pads formed at the extending portion.

17. (new): The stacked semiconductor device as claimed in claim 16, wherein:

the second semiconductor chip is connected by wire bonding to second bonding pads formed on the upper circuit board; and

the second bonding pads are connected to the first bonding pads via a wiring pattern formed on the upper circuit board.

18. (new): The stacked semiconductor device as claimed in claim 11, wherein the upper circuit board comprises an extending portion extending toward a periphery of the upper circuit board, and the extending portion comprises an end surface that is exposed in a side surface of the packaged semiconductor device.

19. (new): The stacked semiconductor device as claimed in claim 18, wherein the end surface of the extending portion is a cut surface formed by cutting so as to individualize the stacked semiconductor device.

20. (new): The stacked semiconductor device as claimed in claim 11, wherein a conductive layer is provided on a substantially entire surface of the upper circuit board opposite to a surface provided with the second wire bonding terminals.